ECE 652
Advanced Topics in Digital Communications
Computer Simulation Project

Part II: *Delta Sigma Modulation*

A second order Delta Sigma Modulator is provided in the directory ECE652/DELTASIGMA. Attached you will find the topology in both graphical and text form.

In the modulator, the Delta Sigma oversampling rate is 2.048 MHz. The baseband bandwidth is 4 kHz. The sinusoidal input is encoded into the bit stream p(k). This bit stream (+- Delta) is filtered and decimated by the integrate and dump (intdmp) star. The decimated sampling rate is 2.048MHz/128= 16 kHz.

These samples are filtered at the low rate of 16 kHz by the IIR filter which has a cutoff frequency of 4 kHz. The SDR star measures the signal to distortion ratio.

Tasks:

(1) Simulate the circuit and plot the Signal to Noise Ratio as a function of input amplitude in dB starting from -50 dB to 0 dB where 0 dB corresponds to an amplitude of 1 volt.

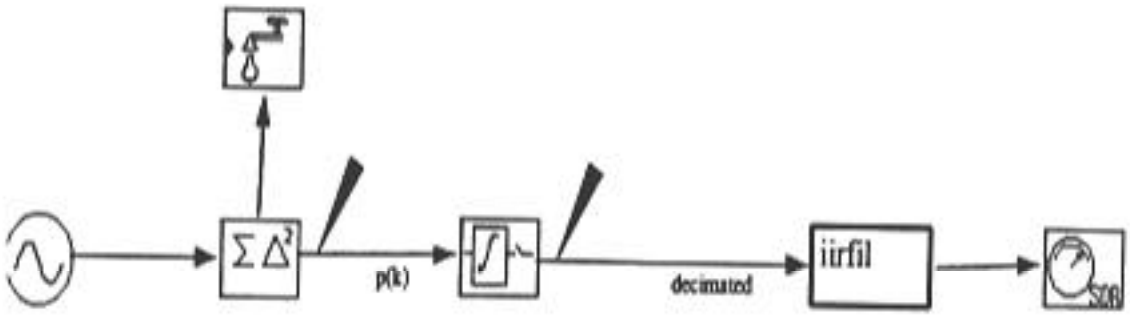
(2) Plot the spectrum of p(k) and the decimated samples and analyse your results for an input amplitude of 0.5 at 2000 Hz. Explain the spectrum and noise you observe.

(3) Evaluate the effect of changing the first loop gain of the delta sigma modulator in terms of the noise shaping of the spectrum and SNR.

(4) Analyze the effect of increasing the sampling rate on the SNR. Note that you may have to change other parameters in the circuit. Use carefull judgment. The sampling rate is set in the *sine* star. You have to change the sampling rate of the IIR filter to fs/128.

(5) Setup a linearized third order loop and verify the theory in class on the stability of the third order loop and the gains at which it will oscillate. Use the integrate star, gain star, and also include a delay star in the feedback loop.

Good luck.



ECE 652
Digital Communications
Project 1 (part 2)
Sigma Delta Modulators

William Farlow

Due: Tuesday, November 12, 1991

Introduction

Sigma Delta (S/D) Modulators provide a low cost, simple Analog to Digital conversion. However, they are nonlinear and therefore difficult to analyze circuits. This report discusses simulation results of a nonlinear model of a second order S/D Modulator and a linear model of a third order S/D modulator. These circuits are shown in Figures 1 and 2.

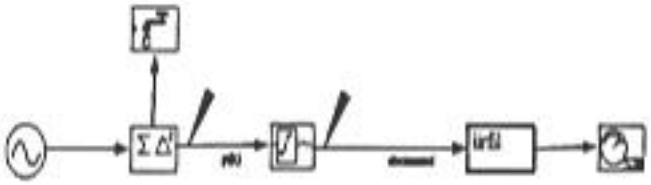


Figure 1: Nonlinear Second Order Sigma Delta Modulator

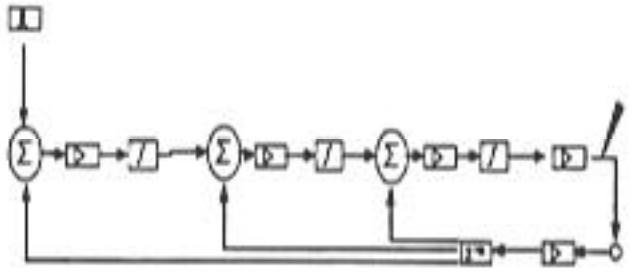


Figure 2: Linear Third Order Sigma Delta Modulator

Question 1

Plot SNR as a function of input amplitude from -50 to 0dB.

In performing this first task, I found a strange phenomena. There seem to be some values of input amplitude that had unexpectedly high/low SNR. While the theory from class and the paper suggests a linear SNR with input amplitude up to saturation, the observed SNR for a 2000Hz input seemed to have phase dependence (not shown here) and also a very jagged line. See Figure 3. Perhaps this can be attributed to the fact that the Sampling Rate and the Signal frequency are related. i.e. $\frac{F_S}{F_{signal}}$ = integer. This relationship makes samples of each cycle identical. When a frequency of 2022Hz was simulated the results were closer to the theory.

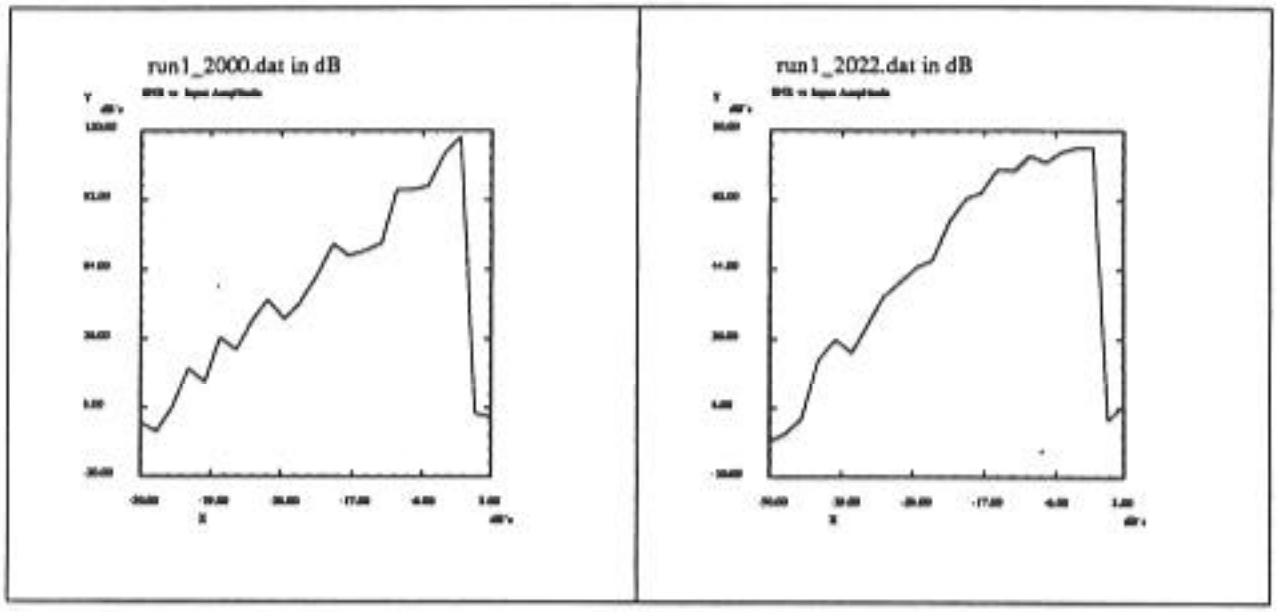


Figure 3: SNR vs Input Amplitude for 2000Hz and 2022Hz

Question 2

The spectrum of P(k) and the Decimated Signal are shown in Figure 4. The spike at 2000Hz is due to the input signal. The high frequency noise is due to the instantaneous error that is produced by the 1bit Quantizer. The average of P(k) $\Rightarrow$ x(k). But instantaneously there are quit large errors due to single bit quantization.

Question 3

As α_1 increases the noise moves in band. Figure 5 shows the corresponding SNR as α_1 increases. The effect of the noise moving in band is obvious. Figures 6 and 7 show the output signal and the P(k) spectrums. When $\alpha_1 \Rightarrow 1$ the noise moves into the base band and distorts the signal.

Question 4

Analyze the effect of increasing the sampling rate on the SNR.

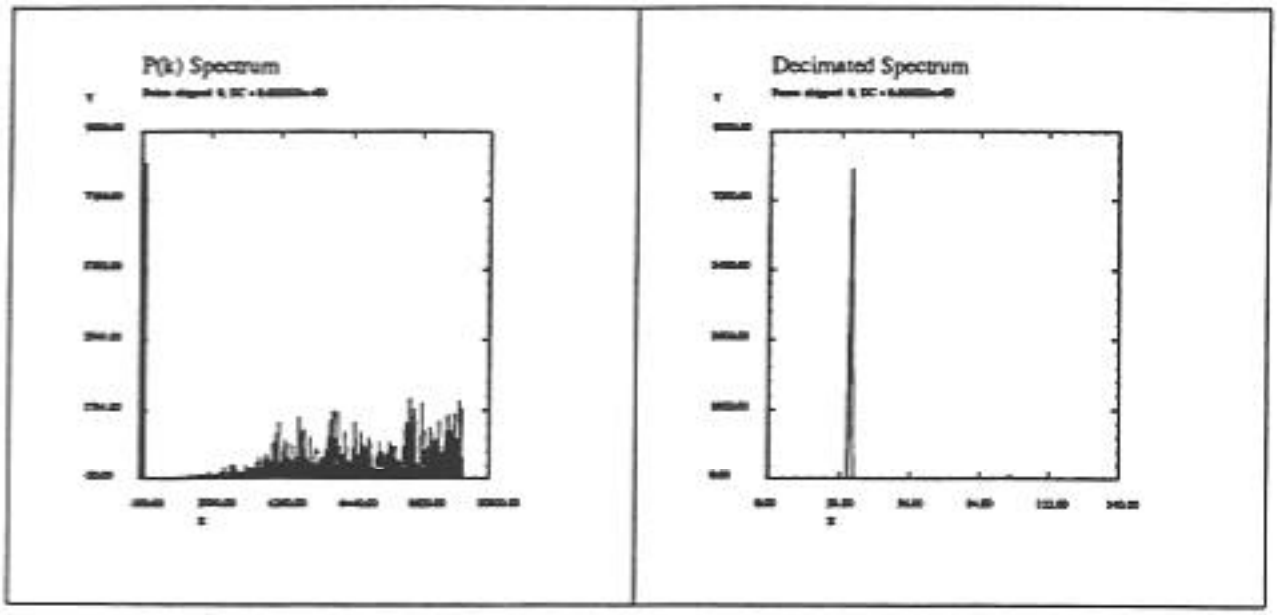


Figure 4: P(k) Spectrum and Decimated Spectrum

From the paper we expect:

$$\text{SNR} = \frac{25\sigma_x^2\alpha_1^2[\alpha_2 K_n]^2}{16\pi^4\sigma_n^2}\frac{f_s^5}{f_b^5}$$

Which leads to a 15dB increase in SNR for doubling f_s. Figure 8 shows the observed SNR vs. Sampling Frequency. While the shape of the curve is similar to the expected, the SNR did not increase at a rate of 15dB per doubling of f_s.

Question 5

From the paper and lectures we expect the the conditions for stability to be:

$$\frac{\alpha_1}{\alpha_3[1+\alpha_1]} \leq \text{K} \leq \frac{8}{\alpha_3[4+2\alpha_2+\alpha_1\alpha_2]}$$

Choosing $\alpha_1 = 0.1$, $\alpha_2 = 0.1$, and $\alpha_3 = 1$ leads to a stable region $0.090909 \leq \text{K} \leq 40$. Figures 9 and 10 show these two bounds. The frequency of oscillation for the lower bound of K is:

$$\sin^2(\omega T_s/2) = \alpha_1\alpha_2/4$$

Figure 11 and 12 show how the oscillating frequency changes with α_2 until α_2 becomes large enough for the upper bound to equal the lower bound. At that point both frequencies of oscillation become equal and there is no stable region. Notice the beat pattern just before the the two frequencies of oscillation become equal.

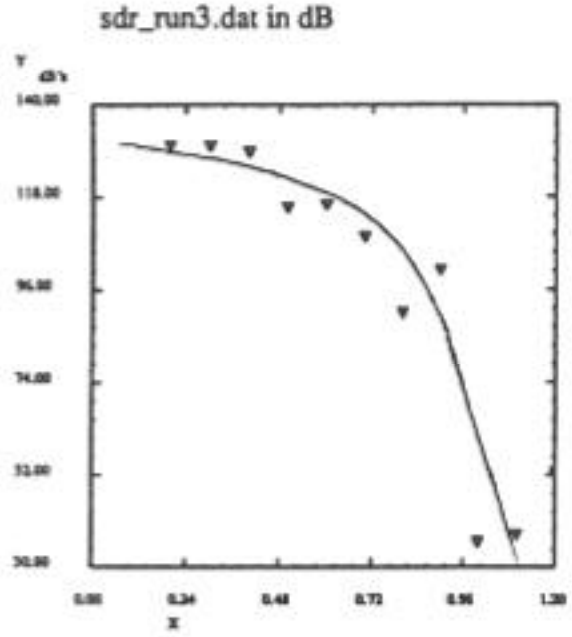


Figure 5: As α_1 Increases, SNR drops

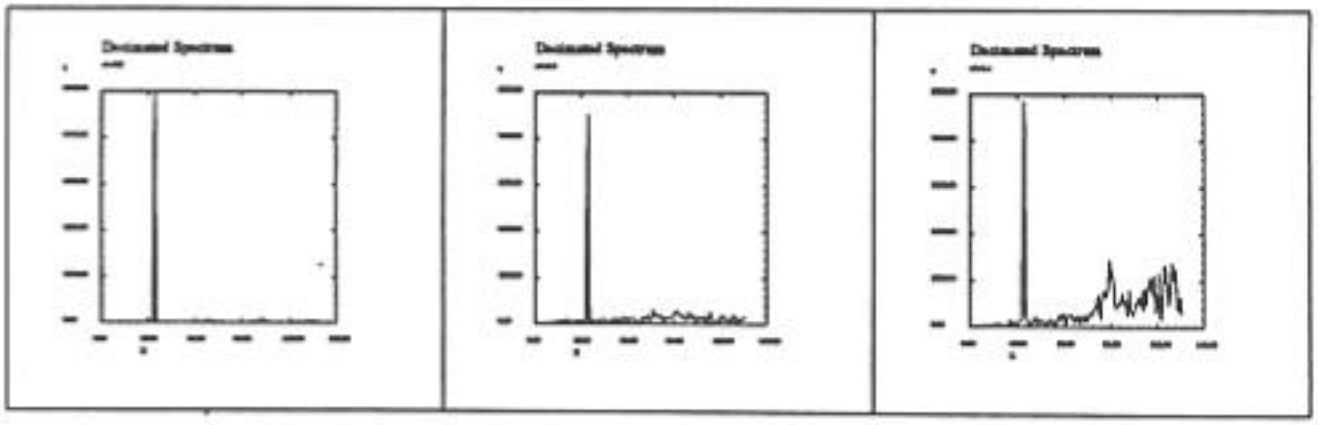


Figure 6: Noise Moves in Band as α_1 Increases

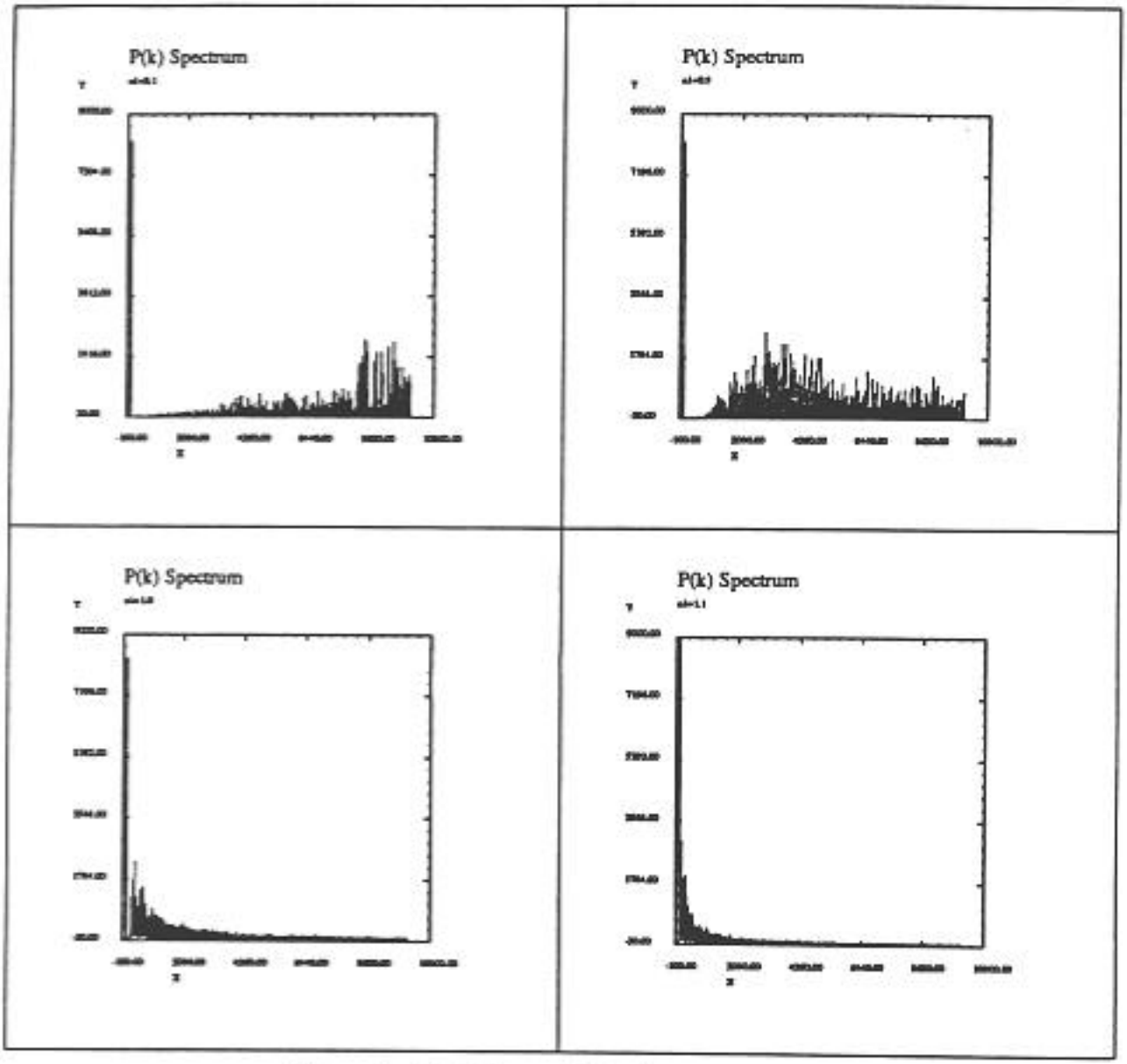


Figure 7: Noise Moves in Band as α_1 Increases

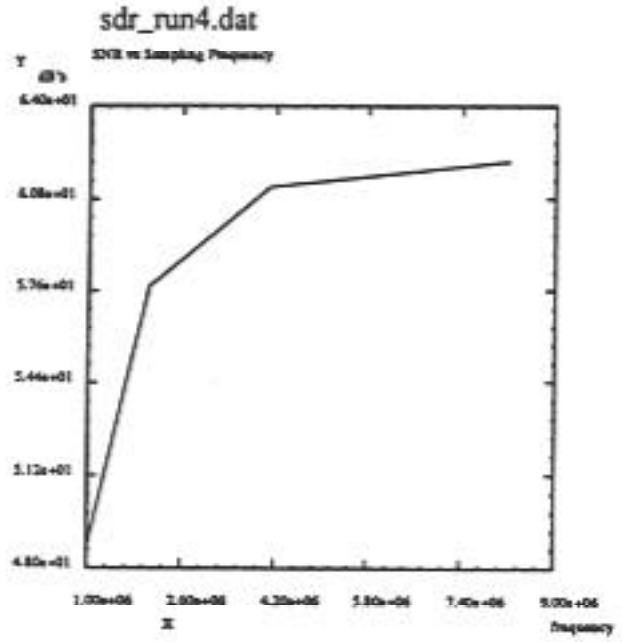


Figure 8: Signal to Noise Ratio vs. Sampling Frequency

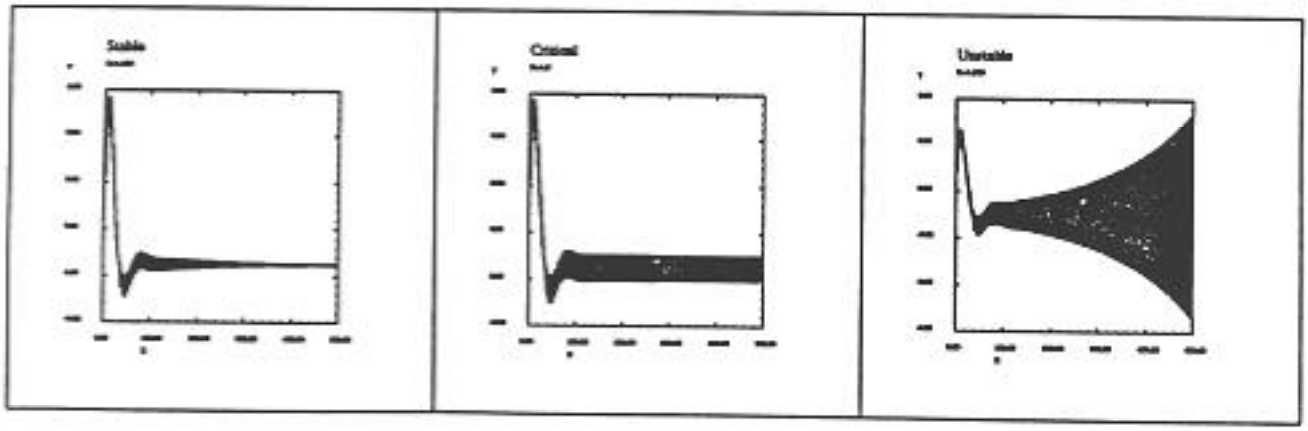


Figure 9: $K \leq \frac{8}{\alpha_3[4+2\alpha_2+\alpha_1\alpha_2]}$

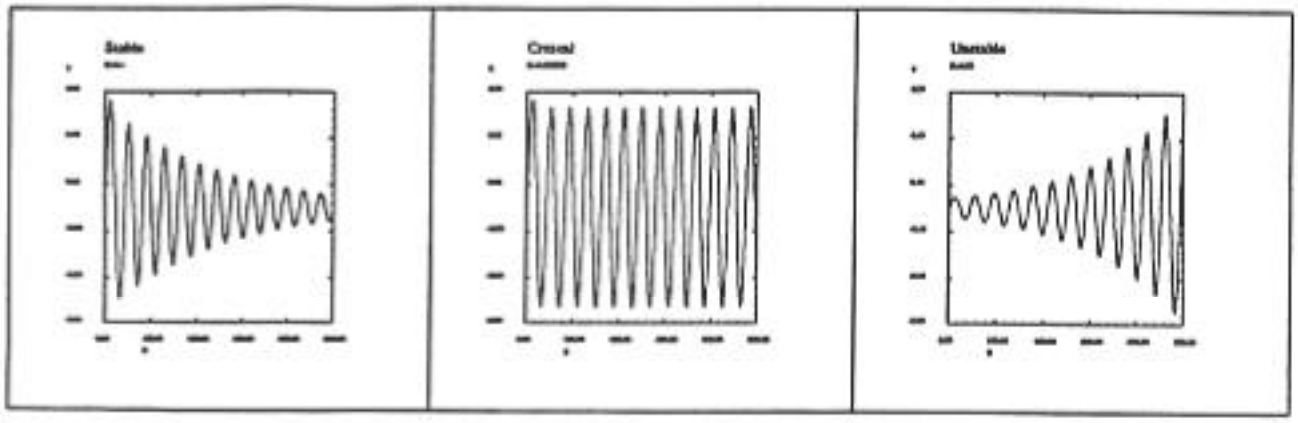


Figure 10: K $\geq \frac{\alpha_1}{\alpha_3[1+\alpha_1]}$

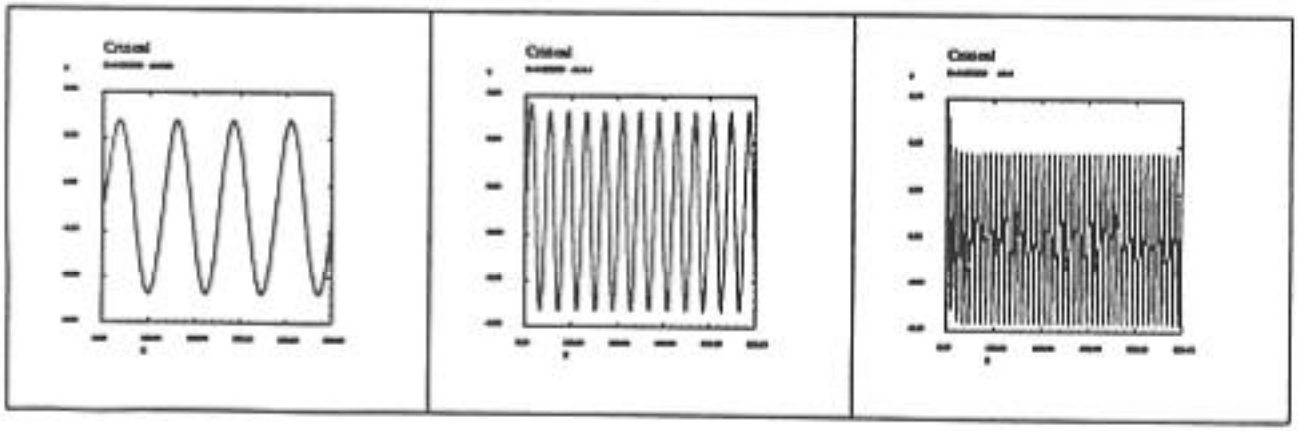


Figure 11: Oscillating Frequency Changes with α_2

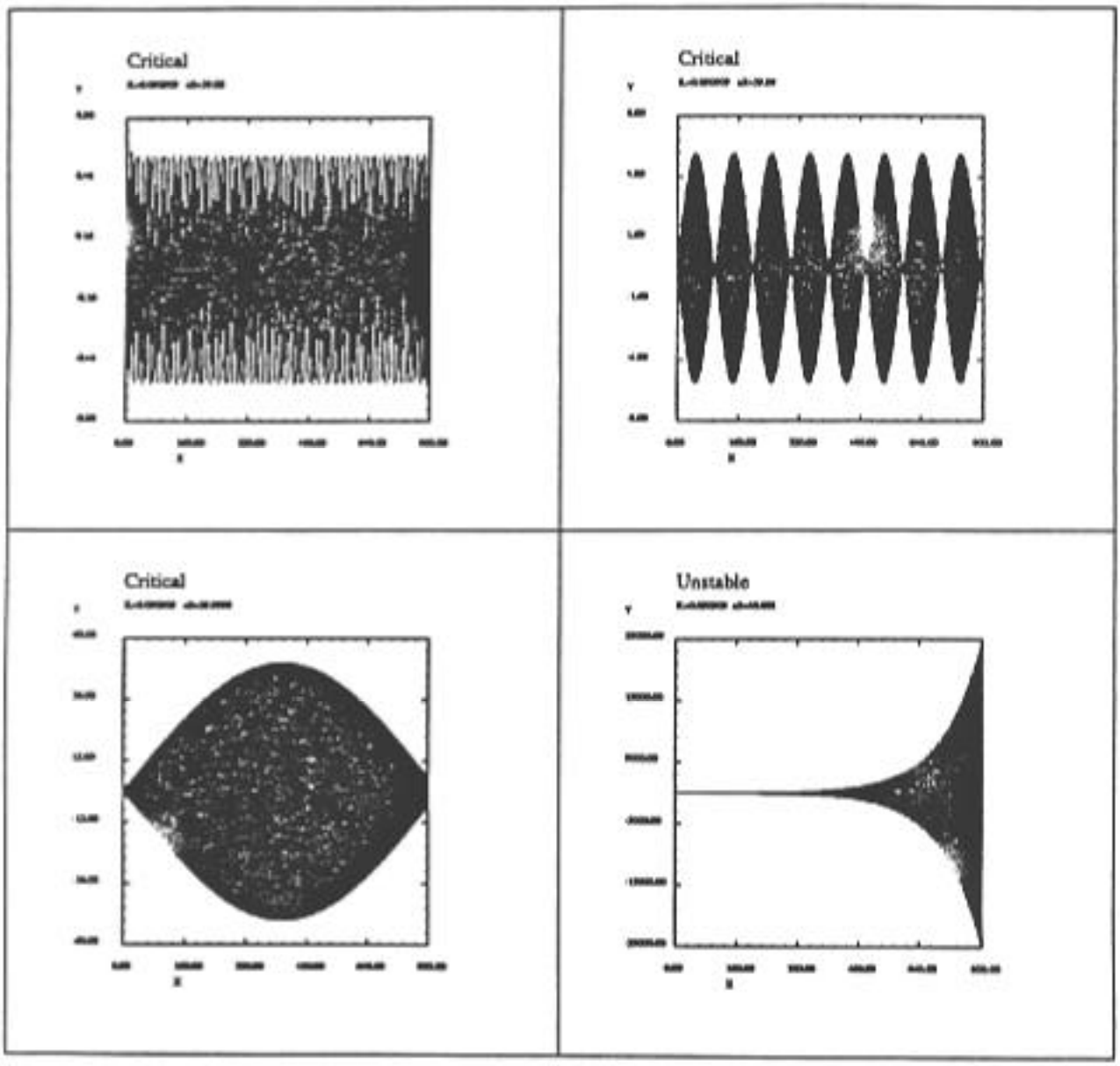


Figure 12: Collapse of the Stable Region as α_2 Increases